TCM 310 IN LOW POWER APPLICATIONS

USING TCM 310 TRANSCEIVERS IN BIDIRECTIONAL LOW POWER APPLICATIONS

11 September 2026

Observe precautions! Electrostatic sensitive devices!

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TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1 Introduction

The TCM 310 is a bidirectional EnOcean transceiver module for gateway applications. Its default firmware is called GatewayController and it uses the EnOcean Serial Protocol 3 (ESP3) on its serial interface [2].

Most TCM 310 applications are line powered. The module works as a receiver or transceiver that never sleeps, so the receiver stays switched on and the module draws more than 33 mA at 3 V continuously. A feature that is rarely used in transceiver designs is the deep sleep mode. The TCM 310 has an internal watchdog and can be set to an energy saving mode with the ESP3 COMMON_COMMAND CO_WR_SLEEP. In deep sleep the current consumption of the module drops below 0.3 µA, which is more than five orders of magnitude lower than in normal operation. This application note explains how the deep sleep mode is used in a bidirectional low power design. It also shows an example circuit that disconnects the serial interface while the module sleeps, so that no residual current flows through the I/O pins of the module.

1.1 References

[1] TCM 310 / TCM 310U Transceiver Gateway Module, User Manual, EnOcean GmbH

[2] EnOcean Serial Protocol 3 (ESP3), Technical Specification, EnOcean GmbH

[3] Dolphin Core Description, EnOcean GmbH

All referenced documents are available in their current version at www.enocean.com.

2 Deep Sleep Mode of the TCM 310

2.1 Entering Deep Sleep

The module enters deep sleep when it receives the ESP3 COMMON_COMMAND CO_WR_SLEEP over its serial interface. The command carries the requested sleep period in units of 10 ms. Table 1 shows the structure of the command packet.

Table 1 Structure of the ESP3 command CO_WR_SLEEP

Group	Offset	Size	Field	Value (hex)	Description
-	0	1	Sync byte	0x55	-
Header	1	2	Data length	0x0005	5 bytes
	3	1	Optional length	0x00	0 bytes
	4	1	Packet type	0x05	COMMON_COMMAND
-	5	1	CRC8H	0xnn	Checksum of the header
Data	6	1	Command code	0x01	CO_WR_SLEEP
	7	4	Sleep period	0x00nnnnnn	Sleep period in units of 10 ms. 0x00000001…0x00FFFFFF (max. ~46 h). After waking up, the module generates an internal reset
-	11	1	CRC8D	0xnn	Checksum of the data

The module answers the command with the ESP3 return code RET_OK (0x00) and then enters deep sleep for the requested period. When the period has elapsed, the module performs an internal hardware reset and starts up again.

2.2 Behavior During Deep Sleep

While the module is in deep sleep it can neither receive nor transmit. This applies to the radio interface as well as to the serial interface. The only ways to leave deep sleep are the internal watchdog and a supply-on reset (SOR).

Note: Current TCM 310 firmware versions are optimized for low energy consumption. From firmware version GATEWAYCTRL 2.11.0.8 (TCM 310 firmware release 14 and higher), the receiver is switched off immediately after the command CO_WR_SLEEP has been received. Because the receiver causes the highest current consumption, this saves additional energy compared with earlier firmware versions.

2.3 Deep Sleep or Supply Switch-Off

Two approaches can reduce the energy consumption between two communication cycles:

- **Switching off the module supply voltage.** No current flows while the module is switched off. However, the cold start-up takes up to 500 ms at the full operating current [1].
- **Keeping the module in deep sleep.** A sleep current of less than 0.3 µA flows. The module is ready for operation again within a few milliseconds.

An energy balance should therefore be calculated for the intended communication interval before one of the two approaches is selected. Frequent communication favors deep sleep, while long intervals between two cycles favor switching off the supply voltage.

3 Application Example: Disconnecting the UART During Deep Sleep

3.1 Use Case

In low power applications such as wireless heating valve actuators, the module can stay in deep sleep most of the time. It wakes up cyclically and only for very short time frames to exchange data with the system. This saves a large amount of energy and allows the device to be powered by a battery or even by an energy harvester.

A typical arrangement uses an ultra-low power microcontroller as the master. The master drives the application, for example a heating valve actuator, and is always powered. The TCM 310 acts as the slave. One communication cycle runs as follows:

1. The module wakes up from deep sleep through its internal watchdog.
2. The module signals that it is ready with the ESP3 message CO_READY.
3. The master exchanges data with the module over the UART. This takes only a few milliseconds.
4. The master sends the command CO_WR_SLEEP with the next sleep period.

5. The module confirms the command with RET_OK and enters deep sleep again.

The circuit described below disconnects the two UART lines while the module sleeps. Without this measure, residual currents can flow from the supply voltage of the master into the unpowered I/O pins of the module and increase the current consumption of the complete system.

3.2 Circuit Description

Figure 1 shows the circuit. Section A contains the TCM 310 as the slave. Section B contains the master. Both sections use the same supply voltage VDD.

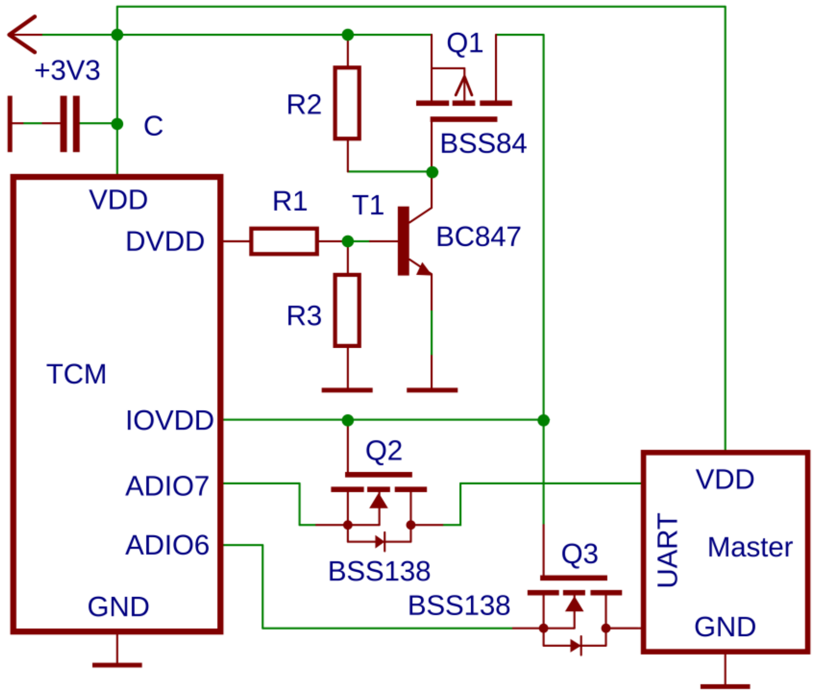

Figure 1 Circuit for disconnecting the UART lines during deep sleep

The circuit consists of two parts:

- **Supply switch for the I/O pins.** T1 and Q1 are driven by DVDD. They connect IOVDD, the supply voltage of all of the module's I/O pins, to VDD during communication and disconnect it afterwards.
- **UART disconnection.** The N-channel enhancement mode MOSFETs Q2 and Q3 work as switches in the two UART lines. The circuit is identical for both lines and is controlled by IOVDD.

The gates of both MOSFETs are connected directly to IOVDD. The sources are connected to the UART lines on the slave side (section A). The drains are connected to the same UART lines on the master side (section B), which is always powered.

Note: In most MOSFETs the substrate is already connected to the source inside the device. If this is not the case, the connection must be made externally. The circuit relies on the intrinsic diodes between drain and substrate, which are part of the MOSFET structure. The next section shows how they work.

3.3 Operating States

Four states that have to be considered:

1. **The module sleeps.** DVDD is 0 V. T1 and Q1 are blocked, so IOVDD is not supplied from VDD. The I/O pins of the slave section are in high impedance state. Gate and source of both MOSFETs are in the high impedance state as well, so their gate-source voltage V_{GS} stays below the threshold voltage and the MOSFETs do not conduct. The UART lines on the master side are pulled up to VDD by the internal pull-up resistors of the master. The intrinsic MOSFET diodes are reverse biased and block. Both UART lines are therefore physically disconnected between section A and section B.
2. **The module wakes up and both lines are idle.** The internal watchdog wakes the module up. IOVDD is switched to VDD through T1 and Q1, so the I/O pins of the module are pulled up internally by default. As long as no device transmits, both lines stay HIGH. Gate and source of the MOSFETs are both at VDD, so V_{GS} stays below the threshold voltage and the MOSFETs do not conduct. The intrinsic diodes do not conduct either, because both sides are at HIGH level. The UART lines on the master side are pulled up to the same level by the internal pull-up resistors of the master. Both lines stay HIGH.
3. **The module transmits.** The module pulls its UART line to LOW. The source of the corresponding MOSFET follows LOW, while the gate stays at IOVDD. V_{GS} rises above the threshold voltage and the MOSFET starts to conduct. The master side of the line is now pulled to LOW as well through the conducting MOSFET. The line is LOW on both sides.
4. **The master transmits.** The master pulls its UART line to LOW, for example to send the command CO_WR_SLEEP. The drain-substrate diode of the corresponding MOSFET is now forward biased and pulls the slave side down first. As soon as V_{GS} passes the threshold voltage, the MOSFET starts to conduct and pulls the slave side further down. The line is LOW on both sides.

These four states show that the logic levels are transferred correctly in both directions, independent of which section drives the line. They also show that the UART lines between slave and master are disconnected while the module sleeps, so that no residual current flows from VDD through the I/O pins of the module during this time. The circuit meets the Dolphin Core requirements for the GPIO supply voltage in deep sleep mode [3] and minimizes the current consumption of the system.

3.4 Measured Behavior

Figure 2 shows the behavior of the circuit during the transition into deep sleep in simplified form.

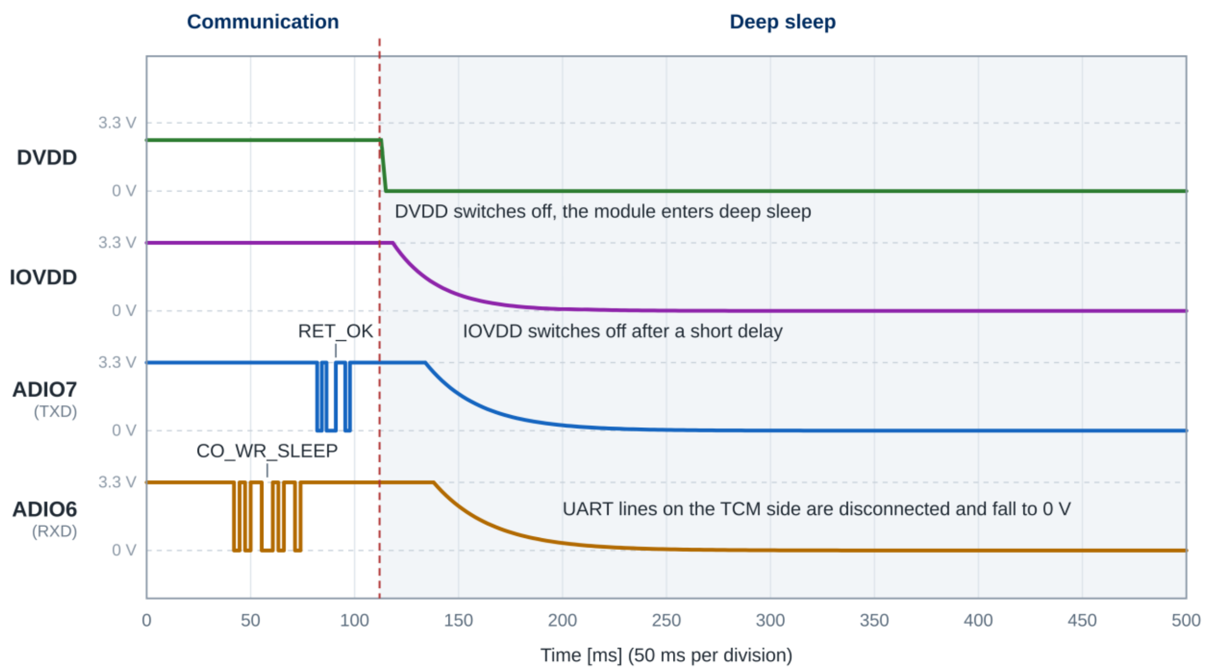

Figure 2 Signals at the transition from communication into deep sleep

Both devices are awake at the beginning. The module receives the command CO_WR_SLEEP from the master on ADIO6 and confirms it immediately with RET_OK on ADIO7. DVDD then falls to LOW, and the module enters deep sleep. IOVDD follows, after a short delay, and the two UART lines on the module side fall to 0 V. The master stays supplied, so the UART paths ADIO6 and ADIO7 remain open during the sleep period of the module.

3.5 Component Selection

- **Common supply voltage.** VDD, and therefore also IOVDD, must be common for both master and the slave, for example +3.3 V.
- **Threshold voltage.** The circuit works properly when the gate-source threshold voltage $V_{GS(th)}$ of the MOSFETs is about 1 V below the lowest supply voltage. If the lowest VDD is +3 V, a threshold voltage of at most 2 V is allowed.
- **MOSFET types.** BSS138 (N-channel enhancement mode) and BSS84 (P-channel enhancement mode) small signal SMD MOSFETs are a good choice, because both have a low threshold voltage.
- **Resistors.** R1, R2 and R3 can be very large. Values from a few MΩ up to tens of MΩ are typical and keep the additional current consumption low.

4 Summary

The TCM 310 can be used in bidirectional low power applications when its deep sleep mode is applied. The command CO_WR_SLEEP sets the module to sleep for a defined period and reduces its current consumption to less than 0.3 µA. The example circuit switches the I/O supply voltage of the module and disconnects the two UART lines during the sleep period. Logic levels are still transferred correctly in both directions during communication, and no residual current flows through the I/O pins of the module while it sleeps. This makes the TCM 310 suitable for battery powered and energy harvesting designs.

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