DOLPHIN Core Description

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EnOcean GmbH
Kolpingring 18a
82041 Oberhaching
Germany

Phone +49.89.67 34 689-0
Fax +49.89.67 34 689-50
info@enocean.com
www.enocean.com

REVISION HISTORY

The following major modifications and improvements have been made to the first version of this document:

No	Major Changes
0.62	Section 2.4.3 added, output currents reduced in 2.4.; Section 3.12 extended
0.7	Tables in 3.3. and 3.4 updated; equivalent schematics added in 2.4.1
0.71	Max. ripple at VDD reduced to 50 mVpp; External 1 kΩ pull-down required at RESET and PROG_EN.
0.8	Additional parameters in 3.11 and 3.4; pull-downs at RESET and PROG_EN changed to 10 kΩ. Description of WXIDIO/WXODIO modified in 2.4.3.
0.81	Max. ratings for PROG_EN added in 3.1 and 3.2
0.82	PROG_EN, RESET, WAKE# added in Digital Input Mode section of 3.11
0.95	Parameter IDD_{OFF} in 3.3 corrected. Parameters of A/D converter corrected and specified in more detail in 3.11. Remarks added regarding use of IOVDD.
0.96	Table in 3.9 updated
0.97	Table in 3.10 corrected. Typ values for FLASH endurance replaced by min values; ESD values added in 3.1; Maximum Rating for IOVDD modified (IOVDD may now exceed VDD); figure added in 2.4.2
1.0	Added 902.875 MHz
1.1	Additional GPIO Parameters, Corrected table for analog output mode on page 26

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www.enocean.com, info@enocean.com, phone ++49 (89) 6734 6890

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EnOcean GmbH
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Germany

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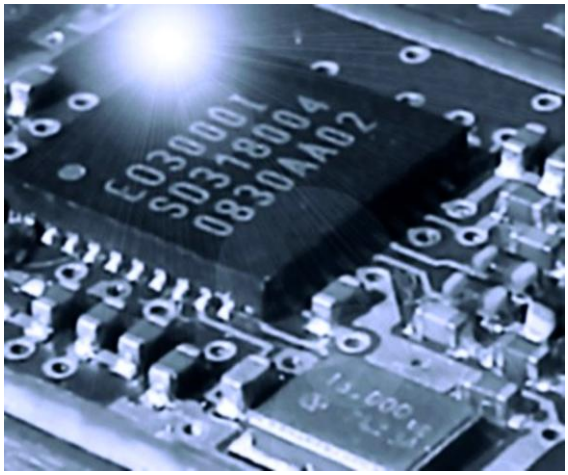
info@enocean.com
www.enocean.com

1 GENERAL DESCRIPTION



DOLPHIN is a complete system-on-chip transceiver solution for bi-directional ultra low power RF applications.
Dolphin is optimized for ultra-low power consumption allowing supply by ambient (harvested) energy.
DOLPHIN comprises an RF transceiver, an 8051 microcontroller core with peripherals and several unique power management blocks.
A SW development environment based on a powerful and flexible API is provided for the development of customer-specific solutions.
This API allows the development of customer specific firmware in C-language and provides functions for chip configuration, transmission and reception of radio telegrams based on the EnOcean radio protocol, ID management, I/O handling, control of power down modes and more.

1.1 Typical Applications

DOLPHIN is designed for use in switches, sensors, actors, receivers and transceivers for building, home, and industrial automation. In a self-powered device configuration it can be powered by various kinds of energy harvesters, such as electro-dynamic energy converters, solar cells, and energy converters for temperature differentials and vibrations.
It can also be used in line-powered devices such as receivers with switched outputs or gateways.

EnOcean GmbH
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Germany

Phone +49.89.67 34 689-0
Fax +49.89.67 34 689-50
info@enocean.com
www.enocean.com

1.2 Technical Data

Frequency (Modulation Type)	315 MHz (ASK)[1] / 868.3 MHz (ASK)[1] / 902.875 MHz (FSK)
Transmit power	programmable -2 to +6 dBm
Receiver sensitivity	-96 dBm (868.300 MHz)[2] -98 dBm (315.000 MHz)[2] -98 dBm (902.875 MHz)[2]
Data rate (transmitter)	125 kbps
Radio protocol	EnOcean
Ultra Low Power Management	typ. 0.2 µA sleep mode with wake up timer
Microcontroller	optimized 16 MHz 8051 µC, 32 kB Flash, 2 kB RAM
Mixed signal sensor interface	14 configurable I/O pins+ 2 wake input pins
Integrated I/O peripherals	4-wire interface, PWM, UART, Schmitt trigger
ADC / DAC	5 channel up to 12 bit / 4 channel 8 bit
Voltage regulators	on chip, 1.8 V also usable for external circuitry
Supply voltage	2 V – 5.0 V, threshold for start-up: 2.6 V
Radio standards	ready for compliance with EN 300 220 and FCC 47 CFR part 15

1) according to ISO/IEC 14543-3-10

2) @ 0.1% telegram error rate (based on transmitted sub-telegrams)

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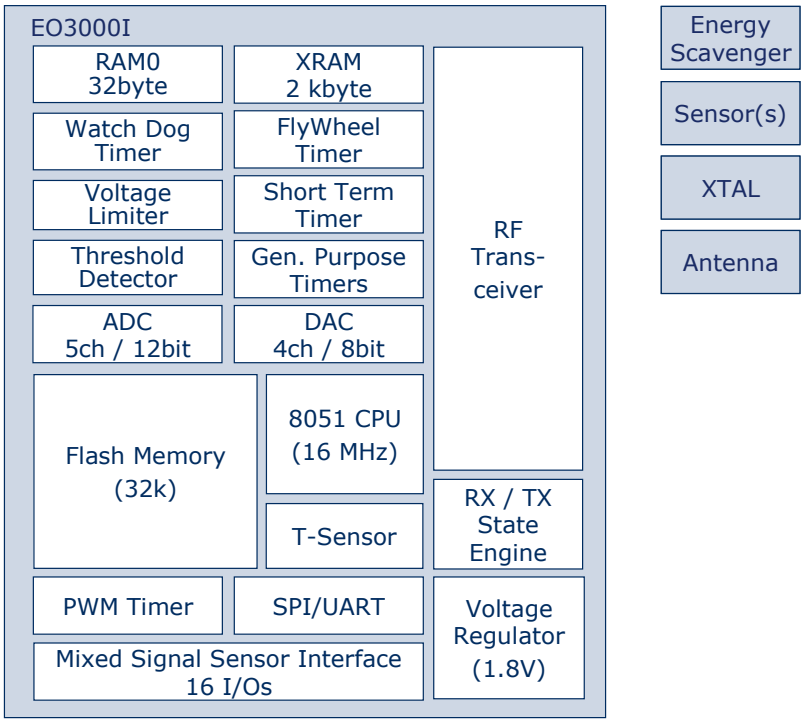
2 FUNCTIONAL DESCRIPTION

2.1 Block Diagram



2.2 Circuit Description

2.2.1 Ultra Low Power Blocks

Voltage Limiter

DOLPHIN provides a voltage limiter which limits the supply voltage VDD of DOLPHIN to a value VDDLIM which is slightly below the maximum VDD ratings by shunting of sufficient current (see section 3.4).

Threshold detector

DOLPHIN provides an ultra low power ON/OFF threshold detector. If VDD > VON, the power distribution and control logic turns on the chip to CPU mode. If VDD ≤ VOFF it initiates the automatic shut down of DOLPHIN by the power distribution and control logic.

Watchdog Timer

DOLPHIN provides an ultra low power watchdog timer based on an internal Watchdog RC Oscillator (WRCO) and programmable digital counter which periodically starts up DOLPHIN by a Supply On Reset (SOR). The watchdog timer cannot be turned off for circuit reliability reasons, but it is resetable by the 8051 CPU to prevent unwanted resets of DOLPHIN.

Continuously supplied RAM0
The special supplied RAM0 is provided for storage of measurement values with comparably low energy effort during "Deep Sleep Mode", and "Flywheel Sleep Mode".
During normal 8051 CPU operation the RAM0 is supplied from DVDD. If DVDD is turned OFF, its supply is connected to UVDD to keep the RAM0 content alive as long as possible. If VDD drops far below VOFF there is no guarantee, but experience shows that the RAM0 content is most probably still valid.

2.2.2 RF Blocks

DOLPHIN provides a configurable RF transceiver part with integrated state machines for the reception (RX) and transmission (TX) of radio telegrams based on the EnOcean radio protocol. 868.3 MHz, 315 MHz and 902.875 MHz protocols used in EnOcean products are available.

2.2.3 Operating Modes

Besides the "OFF Mode" DOLPHIN provides one active mode (CPU Mode) and four standby- and sleep modes. The four standby- and sleep modes use various timers and frequency sources. This allows selecting the most power saving and sufficiently accurate timed operation strategy.

The operating modes in order of increasing energy demand are:

1. OFF Mode
2. Deep Sleep Mode (only UVDD supply regulator running)
3. Flywheel Sleep Mode (only UVDD supply regulator running)
4. ShortTerm Sleep Mode (only UVDD supply regulator running)
5. Standby Mode
6. CPU Mode

Supply On Reset

A "Supply On Reset" (SOR) is executed when VDD raises above VON or whenever one of the following events causes a system reset:

- HW reset (active high HW signal on the RESET input pin)
- SW reset (SW command)
- Watchdog or flywheel-timer time-out

Following an SOR, the 8051 CPU will be clocked by an internal RC oscillator (CRCO) and the default configuration of DOLPHIN will be loaded. DOLPHIN will then enter "CPU Mode".

CPU Mode (Active Mode)

"CPU Mode" is used for system management tasks, preparation for TX and RX, and mixed signal sensor interface activity controlled by the 8051 CPU.
CPU Mode is entered as default configuration after an SOR or configured from ShortTerm Sleep Mode with the 8051 CPU running on the CRCO.
CPU Mode can be also entered from Standby Mode with the 8051 CPU running on the XTO clock source (crystal oscillator).
When the XTO clock has been turned on, is stable running and DOLPHIN is configured for TX, then the CPU may switch on the TX state engine.
Similarly, when the XTO clock has been turned on, is stable running and DOLPHIN is configured for RX, the RX state engine may be switched on.

It is important to prevent DOLPHIN transitioning from "CPU Mode" to "OFF Mode" during writing or erasing of FLASH memory. Failure to do so could result in damage to the FLASH memory and / or data corruption.
Therefore the supply voltage should be measured and the energy budget should be calculated prior to writing or erasing FLASH memory.

The TX state engine can be only used when the XTO clock is stable and the 8051 CPU is running on the XTO clock.
Single data packets (subtelegrams) can be transmitted under autonomous control of the TX state machine. During this transmission, the 8051 CPU may be stopped (standby mode) to save energy. In this case, the selected sleep mode (sleep destination) is initiated at the end of the packet (subtelegram) transmission.
If the 8051 CPU is active during transmission, it may interrupt the transmission via the TX state machine.
DOLPHIN receives consecutive packets (subtelegrams) under autonomous control of the RX state machine. According to configurable conditions, the 8051 CPU may be waked up for management actions or data processing during the receive process.
If the 8051 CPU is active during packet (subtelegram) reception, it may interrupt the RX state machine.

Sleep Modes

Standby Mode

"Standby Mode" is intended for short interruptions of DOLPHIN activity where only the 8051 CPU is stopped to save energy. The CRCO or the XTO clock (if already turned ON) and the CPU timers remain active and all register and memory content remains valid to ensure fastest wakeup and highest timing accuracy at the cost of higher power consumption.
After wakeup from Standby Mode by timer time-out (except watchdog timer or flywheel timer) or external interrupt, all memory and register content is valid and no time consuming initialization is needed. In case of a time-out of the flywheel timer or the watchdog timer, DOLPHIN will execute a Supply On Reset (SOR).

ShortTerm Sleep Mode

"ShortTerm Sleep Mode" is intended for interruptions which are significantly longer than the XTO start-up time (e.g. the pause between subtelegrams).
During Shortterm Sleep Mode, CPU register and RAM content remain valid. Only the TX, RX and synthesizer configuration is lost.
The short term sleep timer is based on a Short Term RC Oscillator (SRCO) clock with moderate accuracy but much lower power consumption compared to the XTO.
Wake-up from ShortTerm Sleep Mode is typically caused by the time-out of the short term timer and resulting in the system entering CPU Mode clocked by CRCO.
At this point, the TX, RX and synthesizer configuration has to be re-initialized before the radio functionality can be used again.

Flywheel Sleep Mode

"Flywheel Sleep Mode" is intended for high precision system timing in low duty-cycle synchronous networks. The flywheel timer is a resettable and pre-settable timer with programmable cycle time and clock divider that is clocked by a wristwatch crystal oscillator (WXTO).
In Flywheel Sleep Mode only the watchdog timer (clocked by RCO), the supply voltage detector, RAM0 and the multi-function flywheel timer (clocked by WXTO) are active. This timer wakes up DOLPHIN periodically for TX or RX activity and timing re-synchronization.
It is also possible to wake DOLPHIN using the WAKE# pins from "Flywheel Sleep Mode".
After wakeup from "Flywheel Sleep Mode" all register and memory content has to be re-initialized.

Deep Sleep Mode

"Deep Sleep Mode" is intended for ambient energy powered, event triggered TX applications, where ultra-low power consumption is mandatory.
In Deep Sleep Mode only the watchdog timer (clocked by RCO), the supply voltage detector and RAM0 are active.
Exit from Deep Sleep Mode can occur either by the time-out of the watchdog timer (to allow periodic system polling) or via a signal on the WAKE# pins. In both cases, a Supply On Reset will be executed and all memory and register content has to be re-initialized.

OFF Mode

DOLPHIN is in "OFF Mode" when the supply voltage is insufficient, i.e. below the VOFF threshold. There is no activity in this mode and DOLPHIN will only consume a very low leakage current. Dolphin will exit this mode once the supply voltage exceeds the VON threshold.

2.2.4 Microcontroller and Peripherals

DOLPHIN contains an 8051 CPU assisted by TX and RX state machines, system timers, CPU timers, and memories as boot ROM, XRAM, FLASH, a specially supplied data RAM0 and the serial interface 0.

The tasks of the 8051 CPU are:
- Initialization of DOLPHIN memory and configuration registers
- Configuration of the radio part
- Configuration of the TX and RX state machines and timers
- Protocol handling of the TX and RX process
- Optional data en- and decoding, en- and decryption, as well as other data manipulation.
- Execution of various user specific applications as e.g. mixed signal sensor interface operation
- Communication with a host processor or peripherals
- Control of self-check of DOLPHIN in the end application or during production (e.g. some kind of loop-back transmission)

For fastest reaction times and minimum energy consumption, the 8051 CPU can be started using the CPU RC oscillator (CRCO) clock and may later switch the clock source to the crystal oscillator (XTO) clock once this clock has stabilized.
The 8051 CPU may communicate with a host processor or its peripherals via the serial interface 0. Serial interface 0 may be switched between SPI and UART operation.
Another serial interface (serial interface 1) with UART operation is available on the mixed signal interface.
An external serial ROM or EEPROM can be connected to the 8051 CPU via the serial interface 0 or the serial interface 1 to provide additional data or program storage.
To allow protection of the program code against manipulation or read out, a part of the internal FLASH memory can be R/W protected by setting a code protection bit.

2.2.5 Mixed Signal Sensor Interface

DOLPHIN supports a mixed signal sensor interface with 10 almost freely configurable I/O lines for:
- Digital control and digital sense by up to 10 configurable digital I/O's
- Output of an analog signal by using an D/A converter
- Sensing of up to two single-ended or differential analog values by using the high performance A/D converters when they are not used by the RX system
- PWM output

The analog functions can be configured to 8 of the 10 I/Os whereas the other 2 I/Os are reserved for wristwatch crystal oscillator operation.
The mixed signal sensor interface configuration is done by a mixed signal I/O interface multiplexer in combination with the function block multiplexers.

2.3 I/O Description and Operational Characteristics

Symbol	Functions	Operational Characteristics
RESET	Reset input Programming Interface (Reset)	Internally supplied by UVDD. Active high reset. External 10kΩ pull-down required.
WXIDIO	Wristwatch XTAL input Slow digital I/O	32 kHz oscillator for flywheel timer max 15 µA output current (UVDD supplied, output available also in deep sleep mode)
WXODIO	Wristwatch XTAL output Slow digital I Optional output of VON signal	32 kHz oscillator for flywheel timer max 15 µA output current (UVDD supplied, output available also in deep sleep mode)
WAKE0	Wake DOLPHIN from Deep Sleep or Flywheel sleep mode Slow digital input	Internally supplied by UVDD.
WAKE1	Wake DOLPHIN from Deep Sleep or Flywheel sleep mode Slow digital input	Internally supplied by UVDD.
UVDD	Ultra low power voltage regulator	Not for supply of external circuitry!
VDDLIM	Voltage limiter input	Parameters defined in 0
VDD	Unregulated supply voltage input	At startup of DOLPHIN VON (see 0) has to be exceeded.
RFN	RF output	
RFP	RF output	
RVDD	RF supply voltage regulator output	Max. 10 mA for external circuitry. See 2.3.1! Switched off while in deep sleep, short term sleep and flywheel sleep mode.
PROG_EN	Programming Interface (Enable programming mode)	HIGH: programming mode active LOW: operating mode External 10kΩ pull-down required.
ADIO0 ADIO1 ADIO2 ADIO3	Analog input Digital I/O	For configuration options see 2.4.1. Supplied by IOVDD
ADIO4	Analog I/O Digital I/O	For configuration options see 2.4.1. Supplied by IOVDD
ADIO5	Analog output Digital I/O	For configuration options see 2.4.1. Supplied by IOVDD
ADIO6	Analog output Digital I/O UART RX	For configuration options see 2.4.1. Supplied by IOVDD Serial interface 1.
ADIO7	Analog output Digital I/O UART TX	For configuration options see 2.4.1. Supplied by IOVDD Serial interface 1.

	Programming Interface (Synchonization output)	
SCSEDIO0	SPI chip select Digital I/O Programming Interface (SPI)	Serial interface 0
SCLKDIO1	SPI serial clock Digital I/O Programming Interface (SPI)	Serial interface 0
WSDADIO2	SPI/UART Write Serial (Input) Digital I/O Programming Interface (SPI)	Serial interface 0
RSDADIO3	SPI/UART Read Serial (Output) Digital I/O Programming Interface (SPI)	Serial interface 0
IOVDD	GPIO supply voltage input	Connect either to DVDD or to supply of external circuits within the tolerated voltage range of IOVDD. See also section 2.4.2.
DVDD	Digital supply voltage regulator output	Max. 5 mA for external circuitry. Switched off while in deep sleep, short term sleep and flywheel sleep mode.
GND	Ground connection	

2.3.1 Using RVDD

If RVDD is used in an application circuit a serial ferrite bead shall be used and wire length should be as short as possible (<3 cm). The following ferrite beads have been tested: 74279266 (0603), 74279205 (0805) from Würth. During radio transmission and reception only small currents may be drawn (I<100 µA).
Pulsed current drawn from RVDD has to be avoided. If pulsed currents are necessary, sufficient blocking has to be provided.

2.4 I/O Configuration

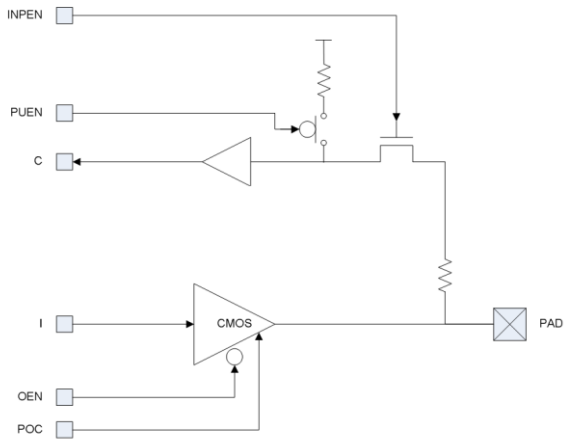
2.4.1 Configuration options

General purpose I/O (GPIO) groups 0, 1, 2 are equipped with I/O pads capable of flexible configurations including tri-state option, programmable pull up resistor, Schmitt trigger input and analog I/O. GPIO2 group pads have lower drive capability, since they are running on the UVDD power domain.

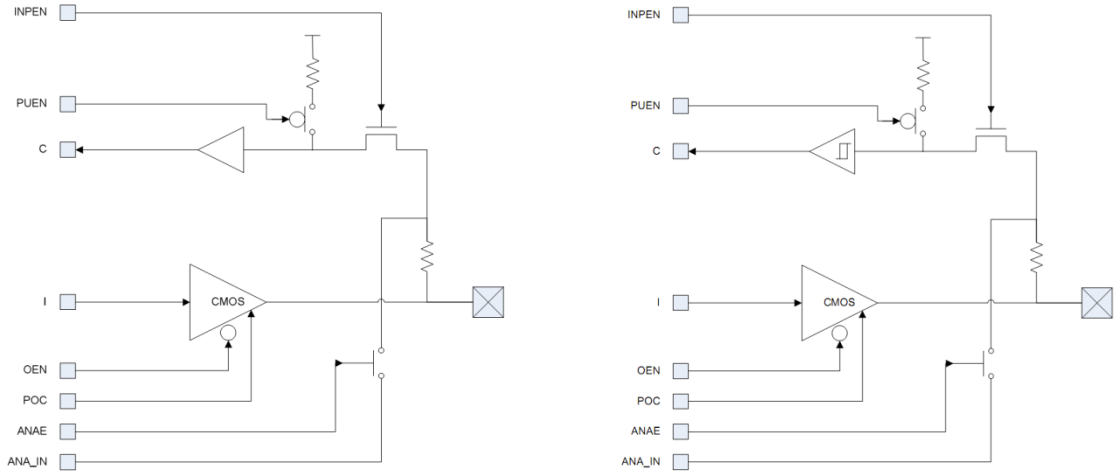
	Name	Power On Config	Digital input configuration: Input Enable	Pull	Direction	Schmitt Trigger	Digital Output	SPI Master	UART	PWM output	Analog	WW XTAL
	RESET	Input pull down										
GPIO 0	SCSEDIO0	Tristate	X	X	Up		X	Chip Select		X		
GPIO 0	SCLKDIO1	Tristate		X	Up		X	Clock				
GPIO 0	WSDADIO2	Tristate		X	Up		X	Data In	I			
GPIO 0	RSDADIO3	Tristate		X	Up		X	Data Out	O			
GPIO 1	ADIO0	Tristate	X	X	Up	X	X			X	I	
GPIO 1	ADIO1	Tristate		X		X	X				I	
GPIO 1	ADIO2	Tristate		X		X	X				I	
GPIO 1	ADIO3	Tristate		X		X	X				I	
GPIO 1	ADIO4	Tristate		X	Up		X			X	I/O	
GPIO 1	ADIO5	Tristate		X			X				O	
GPIO 1	ADIO6	Tristate		X			X		I		O	
GPIO 1	ADIO7	Tristate		X			X		O		O	
GPIO 2	WXIDIO	Tristate	X	X	Up	X	X					I
GPIO 2	WXODIO	Tristate		X	Up	X	VON					O
	WAKE0	Input				X						
	WAKE1	Input				X						

For digital inputs pull-up must be selected!

Input Enable is automatically deactivated when pin is configured as analog.



Equivalent schematic GPIO0: Tri-state option (INPEN), programmable pull-up



Equivalent schematic GPIO1 and 2: Tri-state option (INPEN), programmable pull up, analogue I/O. Schmitt trigger input is available for four GPIO1 pins.

INPEN	Digital input enable
PUEN	Pull-up enable
C	Internal buffered digital input
I	Internal digital output signal
OEN	Digital output enable
POC	Power-on control
ANAE	Analog function enable
ANA_IN	Internal analog signal connection

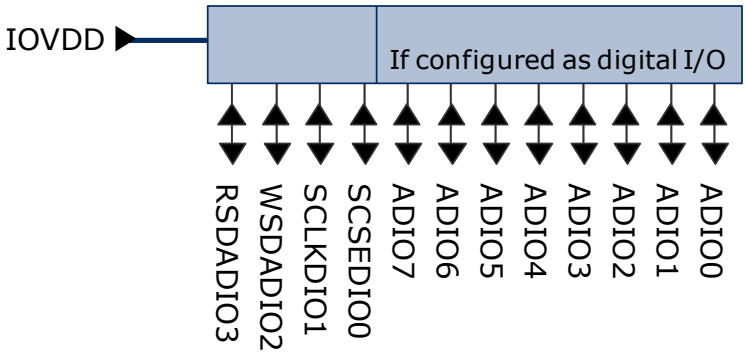
The transistor enabling the input generates a voltage drop. Therefore the voltage measured at the pad is much lower than IOVDD/UVDD (e.g. GPIO0/1: 2.1 V instead of IOVDD=3.3 V; GPIO2: 0.8 V instead of UVDD=1.8 V)!

2.4.2 GPIO supply voltage - IOVDD

For digital communication with other circuitry (peripherals) the digital I/O configured pins of the mixed signal sensor interface (ADIO0 to ADIO7) and the pins of the serial interface 0 (SCSEDIO0, SCLKDIO1, WSDADIO2, RSDADIO3) may be operated from supply voltages different from DVDD. Therefore an interface supply pin IOVDD is available which can be connected either to DOLPHIN´s regulated DVDD or to an external supply within the tolerated voltage range of IOVDD (see 0). Please note that the wristwatch XTAL I/Os WXIDIO and WXODIO are always supplied from UVDD.

If DVDD=0 V (e.g. in any sleep mode or if VDD<VOFF) and IOVDD is supplied, there may be unpredictable and varying current from IOVDD caused by internal floating nodes. Care must be taken to ensure that the current into IOVDD does not exceed 10 mA while DVDD=0 V.
If DVDD=0 V and IOVDD is not supplied, do not apply voltage to any above mentioned pins. This may lead to unpredictable malfunction of the device.

For I/O pins configured as analog pins the IOVDD voltage level is not relevant! However it is important to connect IOVDD to a supply voltage as specified in 0.

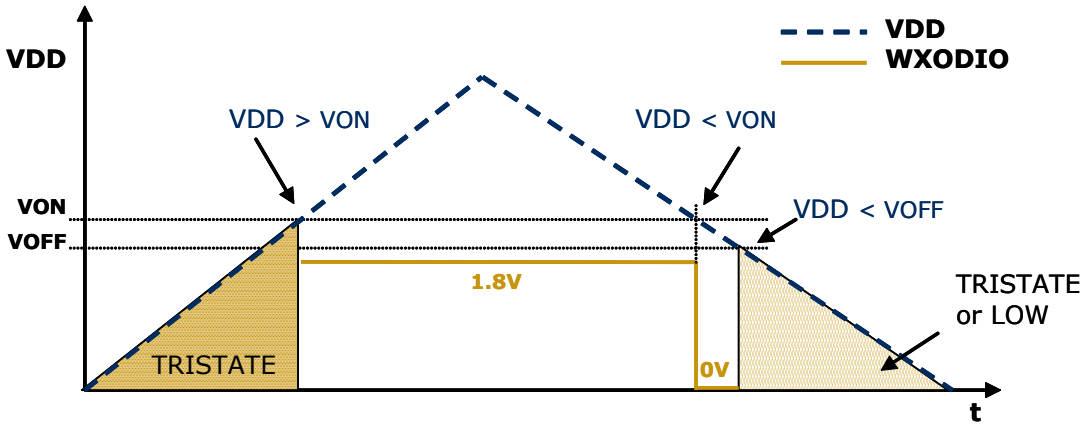


2.4.3 Behaviour of WXIDIO / WXODIO as digital output

WXIDIO can be used as digital output, the output can be controlled by software. WXODIO provides the output signal of the threshold detector for VON when set as digital output. Both pins are supplied by UVDD. The output values remain stable also when Dolphin is in deep sleep mode.

Behavior of WXODIO

- At power up: TRISTATE until VDD>VON then HIGH
- if VDD>VON then HIGH
- if VDD<VON then LOW
- if VDD< VOFF TRISTATE or LOW



Behaviour of WXIDIO

- At power up: TRISTATE until VDD>VON
- VDD>VOFF: Output state according to software control
- VDD<VOFF: Output state stable or TRISTATE

3 RF Parameters and Electrical Characteristics

3.1 Absolute Maximum Ratings (non operating)

Symbol	Parameter	Notes	Min	Max	Units
VDD	Supply voltage at VDD and VDDLIM		-0.5	5.5	V
IOVDD	Supply voltage for GPIO0/1		-0.5	3.6	V
GND	Ground connection		0	0	V
VINA	Voltage at every analog input pin		-0.5	2	V
VIND1	Voltage at digital input pins (GPIO0/1, WAKE0/1, RESET, PROG_EN)		-0.5	3.6	V
VIND2	Voltage at digital input pins (GPIO2)		-0.5	2	V
ESDS	Electrostatic discharge VDD, VDDLIM, UVDD, WAKE0, WAKE1, RESET	according to AEC-Q100-002 (JESD22-A114): HBM: R=1.5 kΩ, C=100 pF	1		kV
ESDN	Electrostatic discharge other pins		2		kV
PTOT	Power dissipation			300	mW

3.2 Operating Conditions

Symbol	Parameter	Notes	Min	Max	Units
VDD	Supply voltage at VDD and VDDLIM		Voff	5.0	V
VDDSLP	Tolerated supply voltage slope	Valid for rising and falling slope	0	5	V/ms
IOVDD	Supply voltage for GPIO0/1		1.7	3.6	V
GND	Ground connection		0	0	V
VINA	Voltage at every analog input pin		0	2.0	V
VIND1	Voltage at digital input pins (GPIO0/1, WAKE0/1, RESET, PROG_EN)		0	3.6	V
VIND2	Voltage at digital input pins (GPIO2)		0	2.0	V

3.3 Current Consumption (excluding output currents via I/Os)

Symbol	Parameter	Conditions / Notes	Min	Typ	Max	Units
IDD_{OFF}	Current Consumption "OFF Mode"	@ VDD=VOFF @ VDD=1 V @27 °C		200 75		nA nA
IDD_{DS}	Current Consumption "Deep Sleep Mode"	@27 °C @85 °C		220 2000	360 3100	nA nA
IDD_{FS}	Current Consumption "Flywheel Sleep Mode"	@27 °C @85 °C		720 2300	1000 4000	nA nA
IDD_{SS}	Current Consumption "Short Term Sleep Mode"	@27 °C @85 °C		8 25	10 35	µA µA
IDD_{SB}	Current Consumption "Standby Mode"	Ultra low power blocks, voltage regulators and XTAL oscillator running		1.4	1.8	mA
IDD_{CPU}	Current Consumption "CPU Mode"	Voltage regulators, XTAL, and CPU 8051 at 16 MHz		3.7	5.1	mA
IDD_{TX}	Current Consumption TX	@868 MHz and +6 dBm TX power during transmission of "H". CPU stopped		23.4	30	mA
IDD_{RX}	Current Consumption RX	@868 MHz CPU stopped		27.4	40	mA

At start-up and after wake-up from deep sleep, flywheel sleep, and short term sleep modes a current peak of up to 600 mA will be drawn for up to 3 µs. This must be taken into account in energy budget calculations and for the design of power supplies!

3.4 Power Management and Voltage Regulators

Symbol	Parameter	Conditions / Notes	Min	Typ	Max	Units
Voltage Regulators						
VDDR	Ripple on VDD, where Min(VDD) > VON				50	mV_{pp}
UVDD	Ultra Low Power supply		1.7	1.8	1.9	V
tUON	Regulator turn on time	At rectangular turn on of VDD from turn on of VDD to regulators active. -40..85 °C -25..65 °C			 50 33	 ms ms
RVDD	RF supply		1.7	1.8	1.9	V
DVDD	Digital supply		1.7	1.8	1.9	V
ΔDVDD% ΔRVDD%	Voltage regulator variation	Over temperature only; related to room temperature			±1.2	%
VBG	Bandgap reference		1.20	1.25	1.30	V
ΔVBG%	Bandgap voltage tolerance magnitude	Over temperature only; related to room temperature			±2	%
Voltage Limiter						
VLIM	Limitation voltage		4.0	4.5	5.5	V
ILIM	Shunting current of limiter				50	mA
Threshold Detector						
VON	Turn on threshold voltage		2.3	2.45	2.6	V
VOFF	Turn off threshold voltage	Automatic shutdown if VDD drops below this level	1.85	1.9	2.1	V
ΔVON_OFF	Difference between turn on and turn off threshold voltage		0.35	0.47	0.59	V

3.5 Frequency Generation

Symbol	Parameter	Conditions/Notes	Min	Typ	Max	Units
XTAL Oscillator						
fXO	XTAL oscillator frequency			16.000		MHz
tXOON	Crystal oscillator startup time		0.7	0.8	1.2	Ms
Wristwatch XTAL oscillator						
fWXO	XTAL oscillator frequency			32.768		kHz
RWXO	Wristwatch XTAL series resistor			50	100	kΩ
ΔfWXO	Relative XTAL frequency tolerance	Depends on application and used crystal tolerance. Oscillator circuit will add typ ~30% to crystal tolerance. Typical crystal tolerance assumed here: 30 ppm		40		ppm
tWXOON	Crystal oscillator startup time			1	10	S
CRCO oscillator (CPU RC oscillator)						
fCRCO	RC oscillator frequency		11.7	16	22.8	MHz
tCRCOON	RC oscillator startup time				1	µs
WRCO oscillator (Watchdog RC oscillator)						
fWRCO	WRCO oscillator frequency			100		Hz
ΔfWRCO	Relative RC frequency tolerance	Uncalibrated One time calibrated			40 10	% %
tWRCOON	RC oscillator startup time			10		Ms
SRCO oscillator (Short term RC oscillator)						
fSRCO	SRCO oscillator frequency			100		kHz
ΔfSRCO	Relative RC frequency tolerance	Uncalibrated Calibrated (Over <100 ms after calibration. Calibration over minimum 200 periods and max. ±1% change of UVDD within this interval.)		40 4		% %
tSRCOON	RC oscillator startup time			10		µs

3.6 Timers

Symbol	Parameter	Conditions/Notes	Min	Typ	Max	Units
Watchdog Timer (supplied by UVDD)						
T_{WDT}	Nominal watchdog interval (24 bit)	At nominal WRCO frequency	0.01		167772	S
ShortTerm Timer (for low power medium-term, medium accuracy applications, supplied by UVDD)						
T_{STI}	Nominal short-term timer interval (16 bit)	At nominal CRCO frequency	0.01		655.35	Ms
Flyweel Timer (for setup of synchronous networks, supplied by UVDD)						
T_{FWT}	Nominal flywheel timer interval (24 bit)	At nominal WXO frequency	0.001		16384	S

3.7 Transmit Operation

Symbol	Parameter	Conditions / Notes	Min	Typ	Max	Units
RTX	Transmit data rate			125		kbit/s
POUT	Typical output power	4 steps, 4 dB each	-2		+6	dBm

3.8 Receive Operation

Symbol	Parameter	Conditions / Notes	Min	Typ	Max	Units
RRX	Receive data rate			125		kbit/s
$S0_D$	Normal receiver sensitivity			-95		dBm

3.9 Serial Interfaces

Symbol	Parameter	Conditions / Notes	Min	Typ	Max	Units
SPI	Data Rate	Configured as SPI Master			2	Mbit/s

Symbol	Parameter	Mode	Nominal data rate kbit/s	Tolerance of nominal data rate	Deviation from desired data rate
UART	Data Rate TX (sent from EO3000I)	"2400" "4800" "9600" "19200" "38400" "57600"	2403.85 4807.69 9615.38 19230.77 38461.54 58823.53	<50 ppm	+0.16% +0.16% +0.16% +0.16% +0.16% +2.12%
UART	Data Rate RX (received by EO3000I)	"2400" "4800" "9600" "19200" "38400" "57600"	2403.85 4807.69 9615.38 19230.77 38461.54 58823.53	<5%	

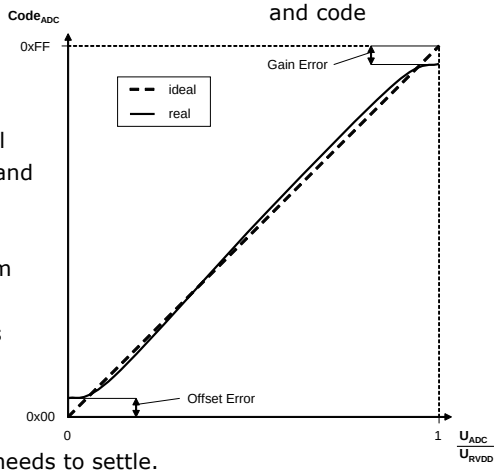
3.10 Microcontroller and Memory

Symbol	Parameter	Conditions / Notes	Min	Typ	Max	Units
Microcontroller 8051						
fUC	CPU 8051 clock speed	With XTO or CRCO as frequency source.		16		MHz
Memory						
	Boot ROM		-	4k*8	-	bit
	XRAM		-	2k*8	-	bit
	RAM0	UVDD supplied	-	32*8	-	bit
	FLASH Size		-	32k*8	-	bit
	FLASH Endurance	@25 °C	20000			cycles
	FLASH Data Retention	@25 °C @85 °C	100 10			years years

3.11 Mixed Signal Interface

Parameter	Conditions / Notes	Min	Typ	Max	Units
Analog Input Mode (ADIO0-4)					
Measurement range	Single ended Internal reference RVDD/2	0.067		RVDD-0.12	V
Input coupling			DC		
Measurement bandwidth[1]			62.5		kHz
Input impedance	Single ended against GND @ 1 kHz	10			MΩ
Input capacitance	Single ended against GND @ 1 kHz			10	pF
Effective measurement resolution			10		Bit
10bit measurement					
Offset error			23	36	LSB
Gain error			32	62	LSB
INL	Code <=200		+3 -14	+6 -23	LSB
	Code >200		+3 -4	+6 -10	LSB
DNL				<±0.5	LSB
8bit measurement					
Offset error			6	9	LSB
Gain error			8	16	LSB
INL	Code <=50		+1 -4	+2 -6	LSB
	Code >50		+1 -1	+2 -3	LSB
DNL				<±0.125	LSB

Offset Error: Describes the offset between the minimal possible code and code 0x00.



Gain Error: Describes the offset between maximum possible code and full scale (e.g. 0x3FF for 10 bit measurements).

Integral Non-Linearity (INL): Describes the difference between the ideal characteristics and the real characteristics. Only values between minimum and maximum possible code are considered (excluding offset error and gain error).

Differential Non-Linearity (DNL): Measures the maximum deviation from the ideal step size of 1 LSB (least significant bit).

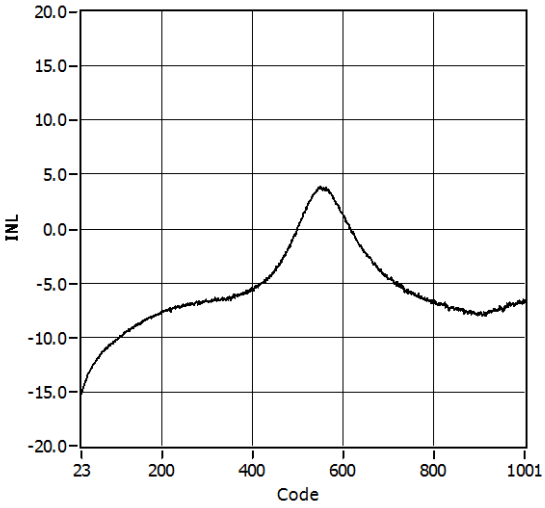
Effective resolution: Results from the signal-noise ratio of the ADC and is given in Bit. The number describes how many bits can be measured stable. The criterion selected here is that the noise of DNL is <±0.5 LSB.

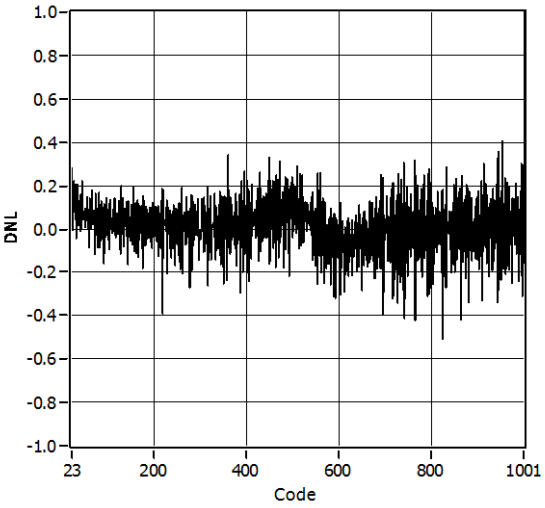
Measurement Bandwidth: The measurement bandwitdh is internally limited by filters. A quasi static signal must be applied as long as the filter needs to settle.
SettlingTime= 1/(MeasurementBandwidth)*ln(2^resolution[Bit])

[1] 3 dB input bandwidth, resulting in 111 µs settling time to achieve a deviation of an input signal <1 LSB (<0.098% @ 10 bit resolution).

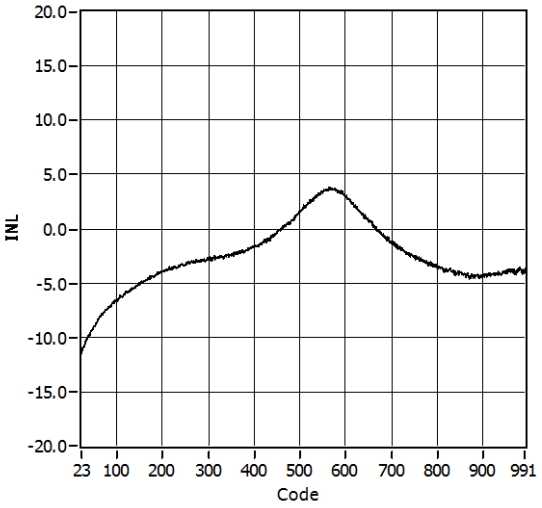
Typical characteristics of INL and DNL (10 bit measurement)

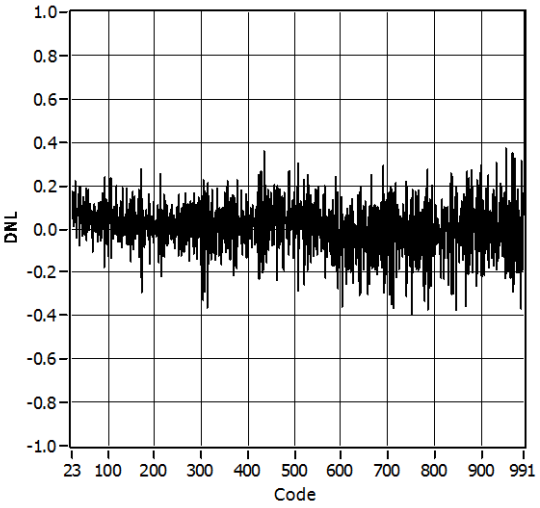
+25°C



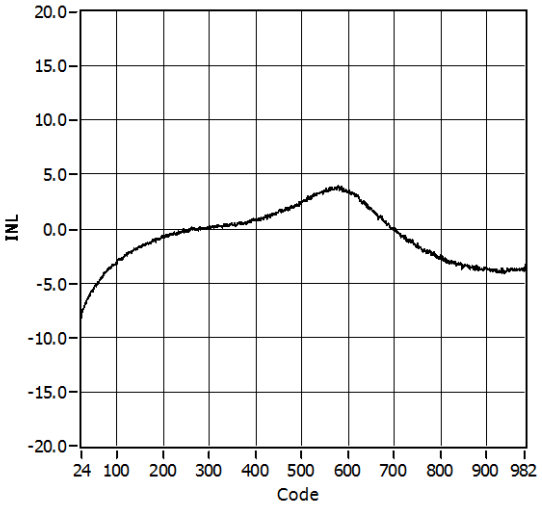


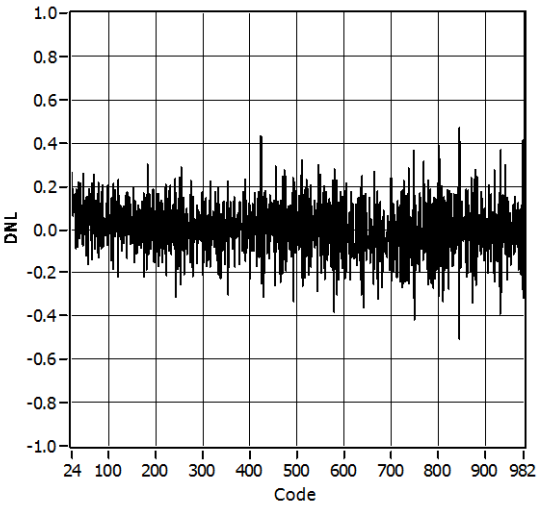
-40°C





+85°C



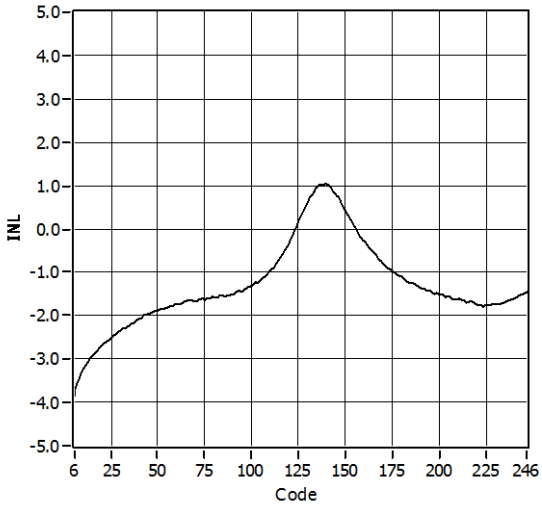


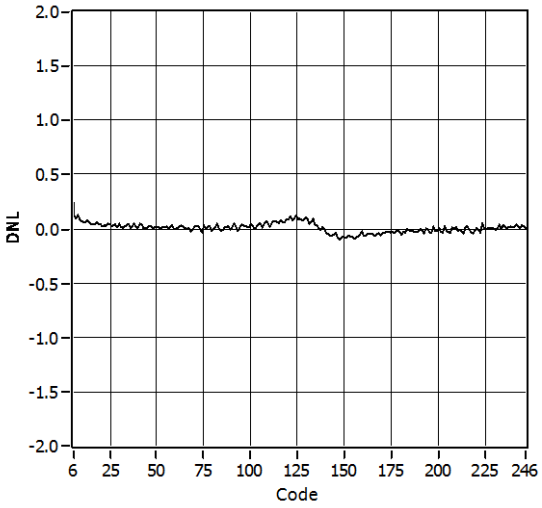
EnOcean GmbH
Kolpingring 18a
82041 Oberhaching
Germany

Phone +49.89.67 34 689-0
Fax +49.89.67 34 689-50
info@enocean.com
www.enocean.com

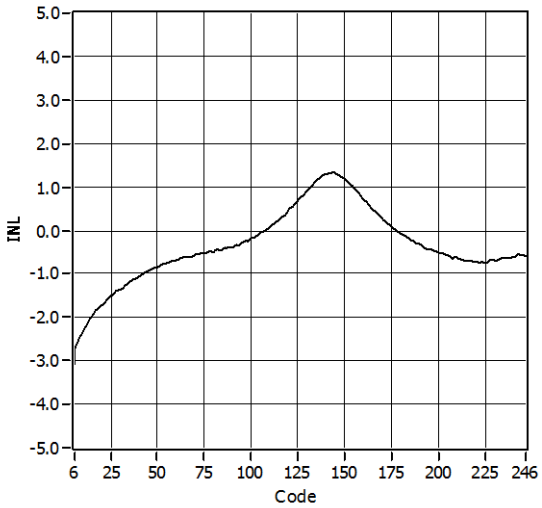
Typical characteristics of INL and DNL (8 bit measurement)

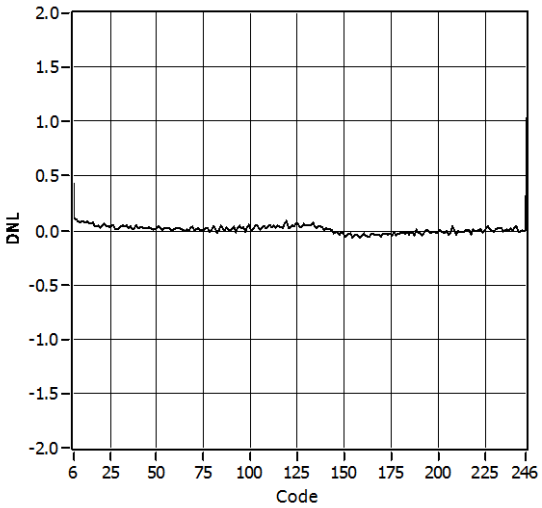
-40°C



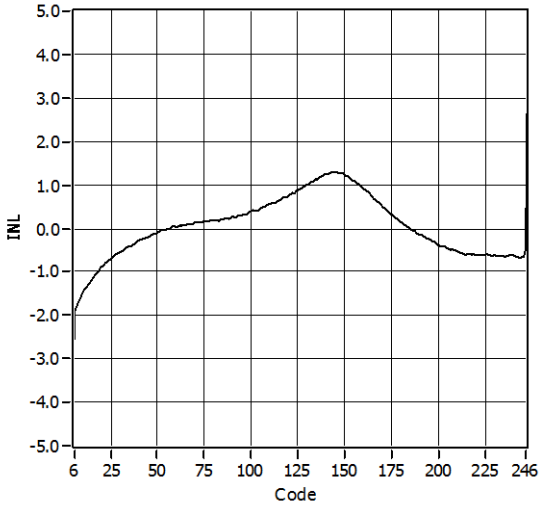


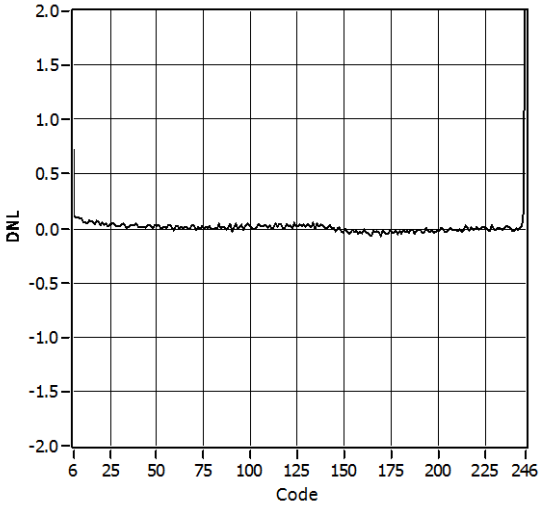
+25°C





+85°C





EnOcean GmbH
Kolpingring 18a
82041 Oberhaching
Germany

Phone +49.89.67 34 689-0
Fax +49.89.67 34 689-50
info@enocean.com
www.enocean.com

Symbol	Parameter	Conditions / Notes	Min	Typ	Max	Units
Analog Output Mode (ADIO4-7)						
	Output range	Single ended	0.05		RVDD	V
	Output coupling			DC		
	Output resistance	Single ended against RGND @ 1 kHz			1	kΩ
	Output resolution			8		bit
Digital Input Mode						
VIH1	Input HIGH voltage GPIO0, GPIO1, PROG_EN		2/3 IOVDD			V
VIL1	Input LOW voltage GPIO0, GPIO1, PROG_EN				1/3 IOVDD	V
VIH2	Input HIGH voltage GPIO2, RESET, WAKE#		2/3 UVDD			V
VIL2	Input LOW voltage GPIO2, RESET, WAKE#				1/3 UVDD	V
	Pull up resistor	@IOVDD=1.7 … 1.9 V	90	132	200	kΩ
		@IOVDD=3.0 … 3.6 V	38	54	85	kΩ
ILZ	Input leakage current		-1		1	uA
ILZG2	Input Leakage Current WXIDIO / WXODIO		-2		2	nA
FGPIO2	Maximum logic speed of WXIDIO/WXODIO pins				1	MHz
	Maximum logic speed of “slow digital” pins	WAKE0, WAKE1			10	Hz
RI	Input resistance	For GPIO0/1/2, no pull resistor enabled	10			MΩ
CI	Input capacitance	For GPIO0/1/2		6	10	pF

EnOcean GmbH
Kolpingring 18a
82041 Oberhaching
Germany

Phone +49.89.67 34 689-0
Fax +49.89.67 34 689-50
info@enocean.com
www.enocean.com

Digital Output Mode						
VOH1	Output HIGH voltage GPIO0 and GPIO1		0.9 IOVDD			
VOL1	Output LOW voltage GPIO0 and GPIO1				0.1 IOVDD	
IOH1	Output HIGH current GPIO0 and GPIO1	IOVDD=3.0-3.6 V IOVDD=1.7-1.9 V			2 0.65	mA mA
IOL1	Output LOW current GPIO0 and GPIO1	IOVDD=3.0-3.6 V IOVDD=1.7-1.9 V			-2 -0.65	mA mA
VOH2	Output HIGH voltage GPIO2		0.9 UVDD			
VOL2	Output LOW voltage GPIO2				0.1 UVDD	
IOH2	Output HIGH current GPIO2				15	µA
IOL2	Output LOW current GPIO2				-15	µA

3.12 Auxiliary Blocks

Internal Temperature Sensor						
	Temperature range		-40		85	°C
	Temperature measure-ment error	When calibrated (offset corrected)			5	K
	Temperature Source	Bandgap voltage with linear tempera-ture behaviour				
	Temperature measure-ment gain	DC offset will vary statistically from device to device		0.725–1.9e-3*T		mV/K